Junction Field Effect Transistors

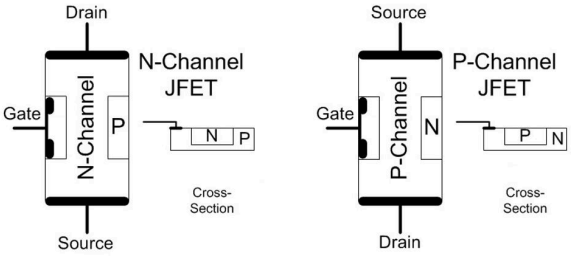
As previously mentioned, JFETs are almost entirely different from BJTs. They would be as different as a mouse and a huge beetle: both have hard skeletons, but one is internal, the other external; both can walk, but there are no similar parts to their legs; even the number of legs is different.

Here's a table of contrasts between the BJT and JFET:

BJT	JFET
Made of three layers	Made of two layers
Two P-N Junctions	One P-N Junction
Hole and Electron Carriers	Hole or Electron Carrier
Normally OFF	Normally ON
Base Current turns ON current	Gate Voltage turns OFF current
Linear Transfer Function	Parabolic Transfer Function
Base, Collector, Emitter	Gate, Drain, Source

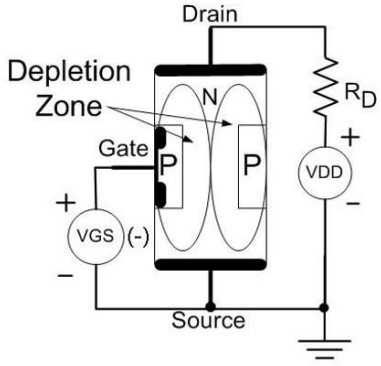
The JFET isn't a very good transistor, and it's not very commonly used. However, in order to understand how FETs work, the JFET is a good starting point. (We're on a journey from a not-very-good transistor to a practically-nonexistent transistor before we can get to the took-over-the-world transistor; so stay tuned!)

Although the JFET has only one P-N Junction, there are three metal connections to the material. Two of them are connected to the opposite ends of one of the types of material, and the third metal connection is to the other material, which is "wrapped around" the other material, as shown below.



FETs use the term "Channel" to describe the path for current through the device, and that makes sense when you look at these block diagrams. The N-Material in the N-Channel JFET is just a good conductor with a metal connection on either end -- ready to conduct if a potential difference is placed across it. That explains why its normal condition is "on". Of course, there will be a depletion region around the P-N Junction that has no carriers in it, which will somewhat narrow the channel, but the channel is open for current flow.

However, if the P-N Junction is reverse biased, the depletion region will get larger, thereby narrowing the channel and restricting current flow. At some point, the depletion region will completely take over the channel, and no further current will flow. That is shown in the following biased diagram of an N-Channel JFET.

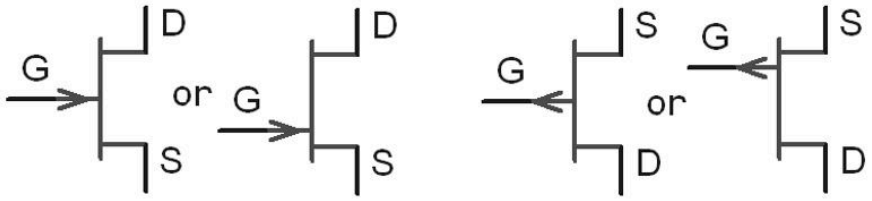


In order for the P-N junction to be reverse-biased, the P material (the Gate) must be at a lower potential than the N-Material in the channel. Of course, when the transistor is conducting, there's not much difference between the two ends of the channel; but when the channel is no longer conducting, there's a big difference. Therefore, we reference the Gate's voltage to the voltage at the Source, and the controlling voltage is called V_{GS}. In this block diagram, V_S is at ground, or 0 V, therefore to reverse bias the P-N Junction, the

Gate voltage must be negative. Since V_{GS} means V_G - V_S, this means that V_{GS} must be negative for an N-Channel JFET. If the P-N Junction was ever forward-biased, it would just turn this device into a very poor diode, since the Gate is not designed to handle any current.

Notice that the labelling convention we used for the BJT carries on here -- a doubled subscript V_{DD} to indicate a power supply that biases the Drain, R_D to indicate a resistor biasing the Drain, and a double subscript V_{GS} to show the difference in potential between two pins on the device.

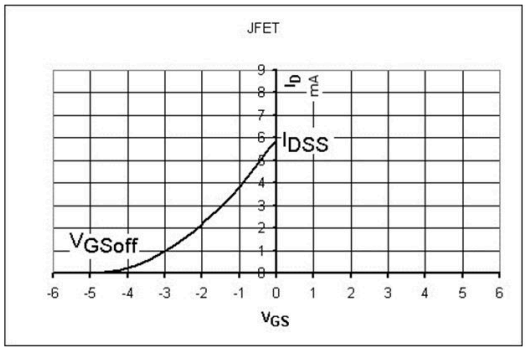
In a schematic diagram, the following symbols are used for JFETs:

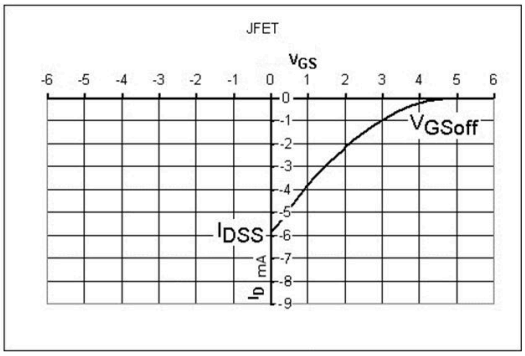


N-Channel JFET P-Channel JFET

The symbols are based upon the construction of the devices: The vertical bar is the Channel, with the metal connections for the Drain and Source attached. The Gate is shown influencing the channel through a P-N junction, where the arrow indicates which material is P and which is N, just as in the diode. Often the Gate is shown closer to the Source to help us remember that V_{GS} is the controlling voltage.

As mentioned before, the Transfer Function for the JFET is non-linear; parabolic, in fact, as shown below.





N-Channel P-Channel

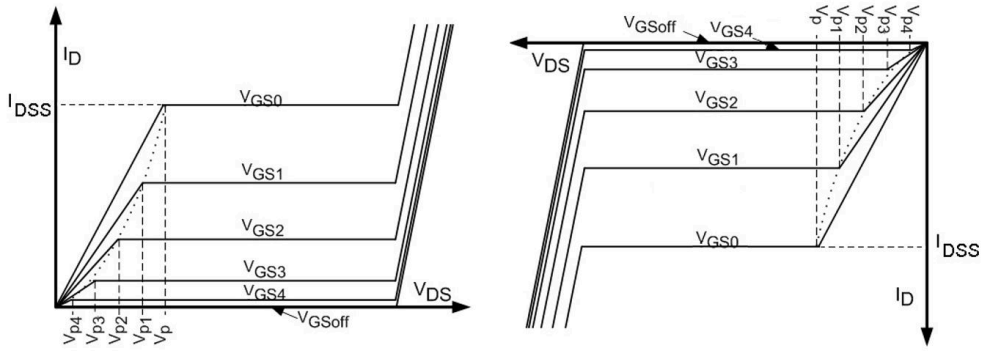
To be more specific, the Transfer Functions are half-parabolas that terminate at two points: V_{GSoff} and I_{DSS}. It probably comes as no surprise that the graphs for the N-Channel devices and the P-Channel devices are inverted to each other. Here's a bit of a summary:

Characteristic	N-Channel	P-Channel
V_{GS} - controlling input voltage	Negative	Positive
I_D - controlled output current	Positive	Negative
V_{GSoff} - voltage at which I_D becomes zero	Negative	Positive
I_{DSS} - maximum current that can flow	V_{GS}=0	V_{GS}=0
Forbidden input voltage range	V_{GS}>0	V_{GS}<0

V_{GSoff} and I_{DSS} are transistor characteristics given in the specification sheet, just as V_{BEon}, α, and β were given for the BJT.

If V_{GS} goes past V_{GSoff}, the transistor remains off -- the parabola doesn't rise up again as it would mathematically. In other words, the parabolic shape only helps us predict voltages and currents between V_{GSoff} and I_{DSS}.

When put on a Curve Tracer that holds V_{GS} constant while increasing the voltage across the transistor, V_{DS}, we get a family of curves similar to those for the BJT, with some very noticeable differences.



N-Channel JFET P-Channel JFET

First, it may be noticeable that the flat lines in the Active Region are really flat, which means that these devices have a very high internal impedance when they are working as Current Sources. That's what JFETs do best -- act as almost-ideal current sources, holding the current constant regardless of the voltage across the device, at least between what's called the "Ohmic Region" and Reverse Breakdown.

Second, the spacing between the different traces isn't constant as it was for the BJT -- it increases in size in proportion to the square of the input voltage.

Third, the voltage at which the device enters the Active Region isn't a tiny little voltage like V_{CEsat} was for the BJT. In fact, V_p could be 2 V, 3 V, even values like 10 V, which doesn't make the JFET a very good switch. Switches are supposed to have essentially zero volts across them.

Finally, the points at which the device enters the Active Region fit into a half-parabola, which just so happens to match the half-parabola in their Transfer Functions.

Questions:

In one JFET circuit, V_G = +10 V, V_S = +10 V, and V_D = 0 V.

1. If this device is wired properly, is it N-Channel or P-Channel? P-Channel
2. V_{GS} = 0 V; would you expect to see maximum current or zero current? maximum cur…
3. Would you have to raise or lower V_G to change the current? raise

In another JFET circuit, I_D is positive.

4. If this device is wired properly, is it N-Channel or P-Channel? N-Channel
5. Would V_{DS} be positive or negative? positive
6. Would V_{GS} be positive or negative? negative
7. To make maximum current flow, if V_S=0, what should V_G be? 0 V